Latent Damage and Reliability in Semiconductor Devices

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Imagine for a moment...

Chicago: Big rough city. 911 calling center is critically important. Quite a bit of investment in an insanely reliable system.

A lightning storm comes one day, and power goes out. Normally it's fine, because they have back-ups. But it ended up failing. Their UPS burned out due to a microcontroller failure. Mass chaos in the city.

Afterward, the company who made the system went in and performed a standard repair procedure: swapping out boards until it works again.

But if Latent damage exists, then the non-replaced boards could fail much sooner than expected.

What is Latent Damage?

Latent Damage:

- Is usually caused by an Electrostatic Discharge (ESD) event
- Physically damages a device
- But is electrically undetectable
- Reduces the lifetime of the device

This is the theoretical definition of Latent Damage.

Does Latent Damage exist?

Some studies show evidence for the existence of Latent Damage, while others don't.

As it stands now, Latent Damage is an ongoing topic of study.

Specifically, we care about Commercial off-the-Shelf (COTS) parts.

If it exists, it will reduce the overall lifetime of COTS devices.

Why should we care?

It has huge implications on Industry, as well as society as a whole.

If it does exist, COTS devices might not be as reliable as the specifications describe.

Unexpected failures increase the cost of repairs on a system.

Latent damage can lead to profit loss.

Hypothesis

If an ESD event occurs on a semiconductor device, then latent damage exists.

This latent damage can cause the reliability of these devices to decrease.

Resulting in the Mean Time to Failure (MTTF) to be shorter than the manufacturing specifications.

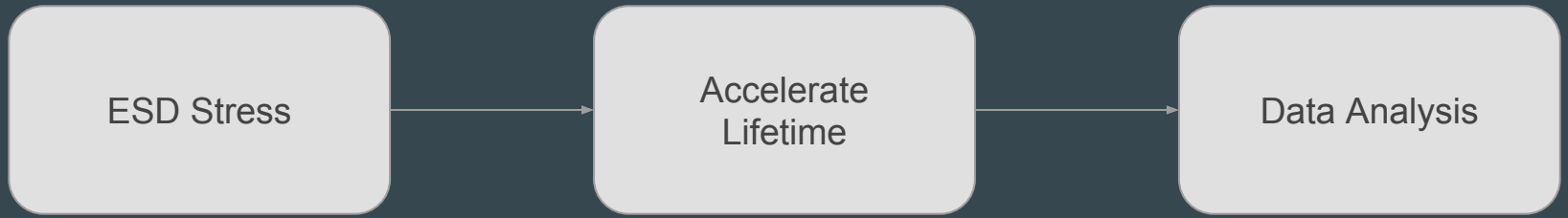
Overall Project Plan

An experiment with three parts:

- Stressing devices
- Burn-in testing
- Data analysis

Some existing work has already been done on this topic here at Iowa State.

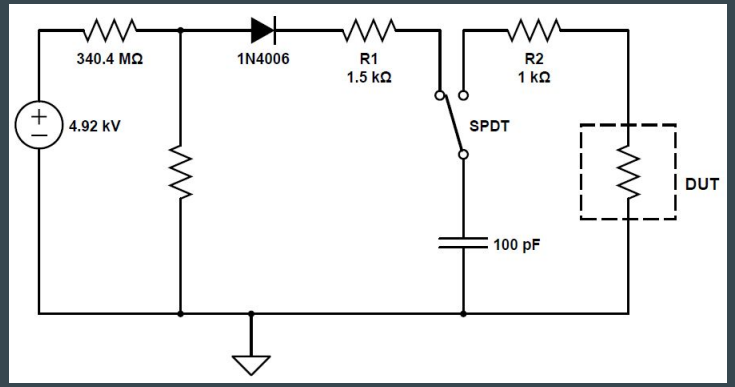
To stay within time and budget constraints we attempted to use/repurpose the existing Printed Circuit Boards (PCBs).



Stressing Devices

General Procedure

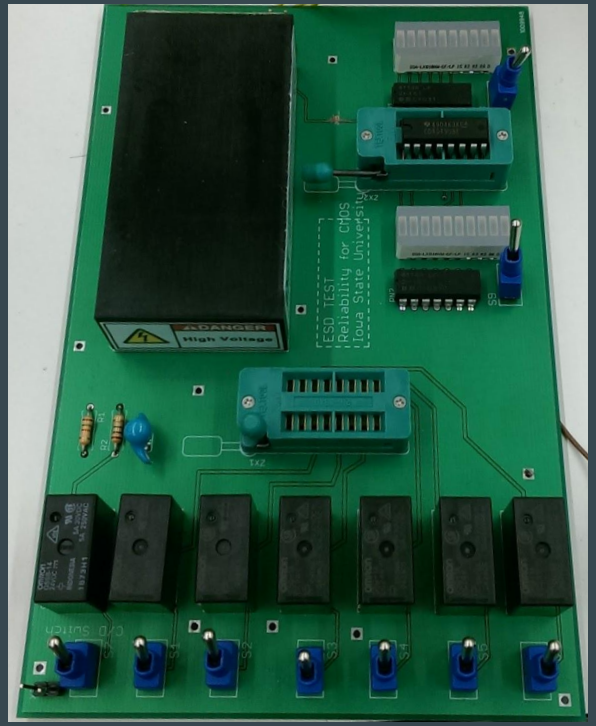
- Devices will be exposed to an ESD event at a high-voltage level
- Human Body Model (HBM)
  - 100pF Capacitor charged to a high-voltage
  - Discharged into Device Under-Test (DUT) with the output tied-low
- Texas Instruments (CD4049UBE)
  - 6 CMOS inverters on one chip (hex inverter)
- Through experimentation, determine a maximum stress level (high-voltage)



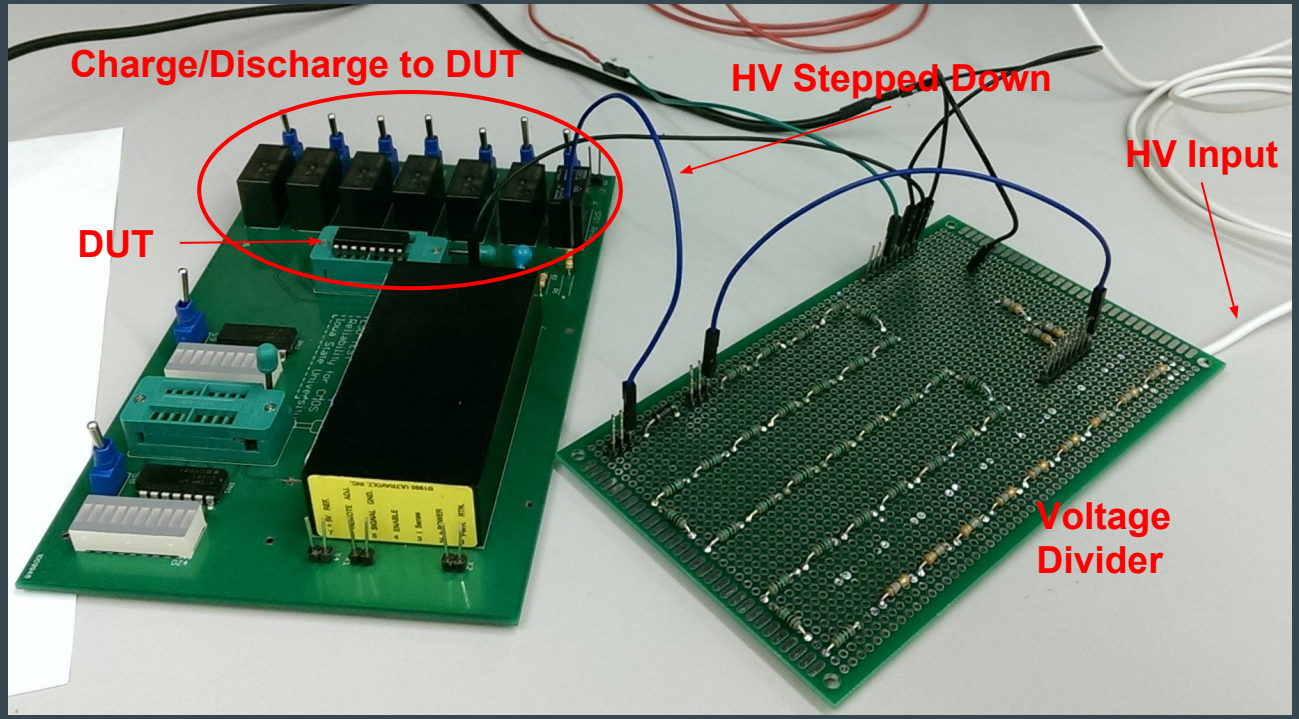
Stressing Board

Existing Work

- An ESD Stress PCB was previously created
  - Simulate an ESD event
  - Functionality check
- Programmable high-voltage source was non-functional
  - Re-purposed the PCB to use an agriculturally purposed high-voltage source



ESD Stress Setup



Burn-in Testing & Oven

General Procedure

Once the parts are stressed, they are put into a burn-in oven.

The burn-in oven is used to accelerate the lifetime of the parts.

While the parts are in the burn-in oven, they'll be conducting current.

These parts will be measured regularly during procedure, to record their lifetime.

Burn-in Boards

Existing Work

10 boards from previous work used for burn-in testing

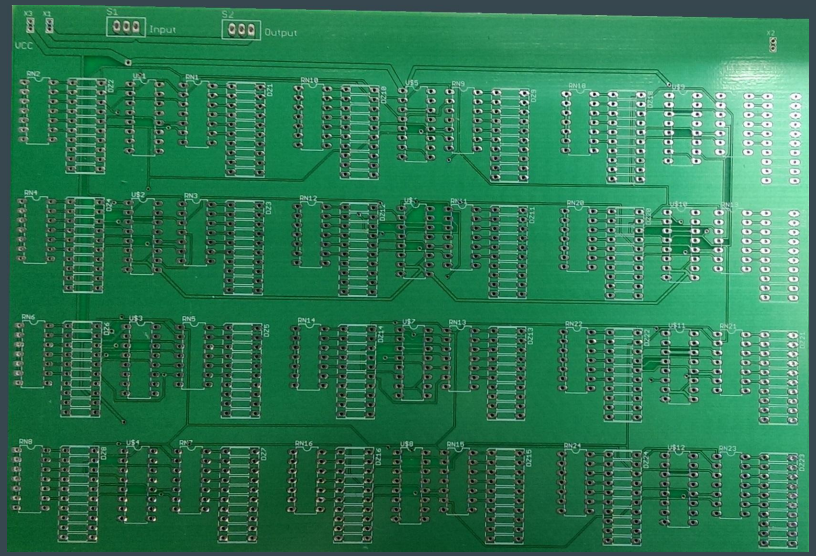
9 boards are populated with the parts in the testing set-up (next slide)

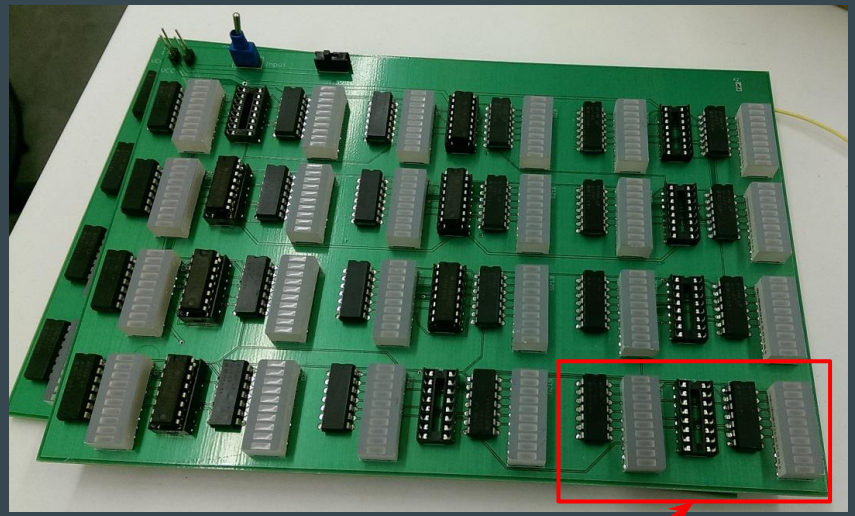
Each board has 12 testing set-ups, one set-up for each part to test.

Serious issues make these boards unusable for our purposes (to be discussed.)

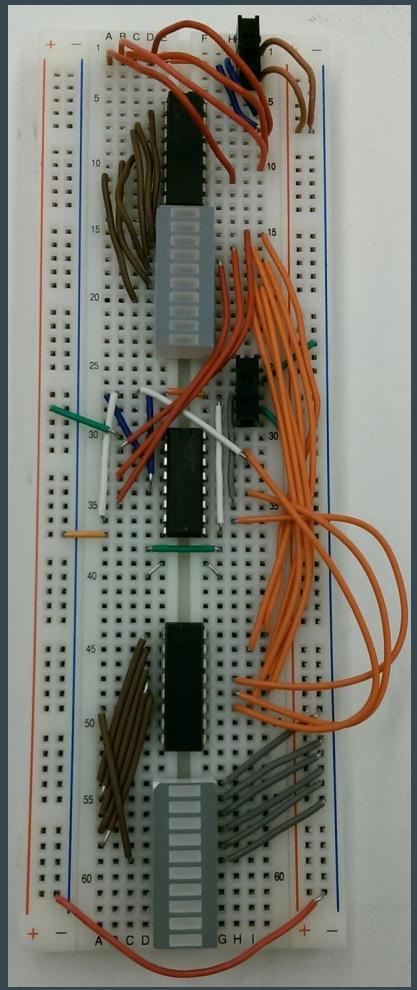
Burn-in Boards

Existing Work



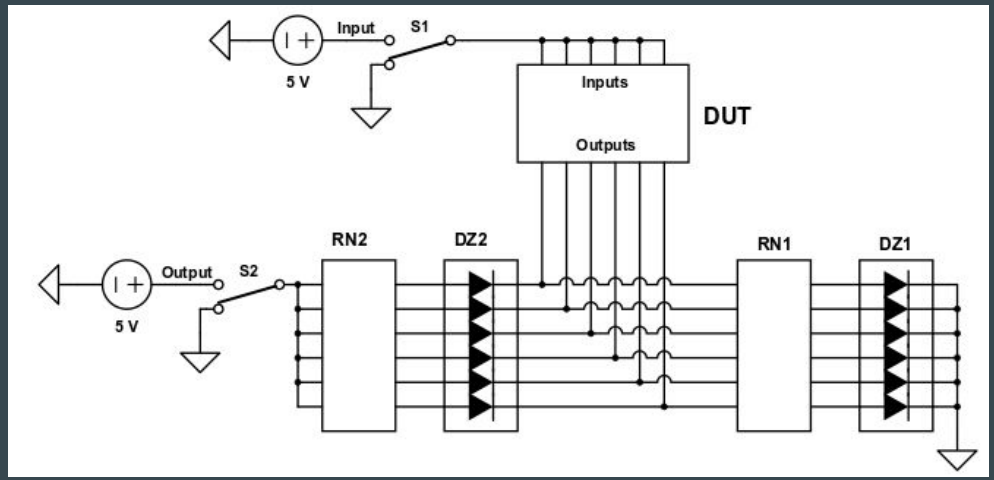


1 Testing Set-up



Functionality Testing

- The bread board on the left is to test a *single* hex-inverter
- The circuit schematic below is what is on that breadboard



Functionality Testing

Truth Table

In the table below, 1 means “high” for the switch states, and 1 means conducting for the components.

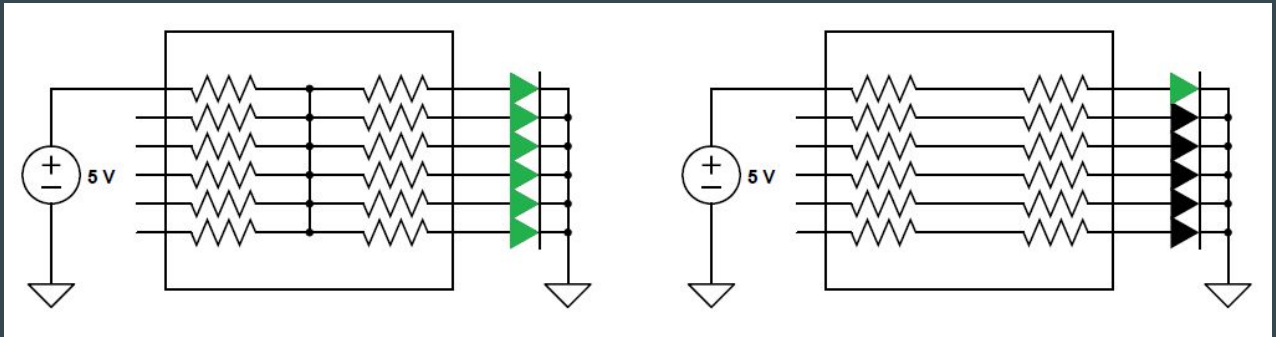
Switch		Diodes		Inverter Transistors	
“Input”	“Output”	DZ1	DZ2	PMOS	NMOS
0	0	1	0	1	0
0	1	1	0	1	0
1	0	0	0	0	1
1	1	0	1	0	1

Burn-in Boards

Issues

There are two major problems with the existing boards:

1. Resistor networks in the testing set-up are bussed instead of isolated.



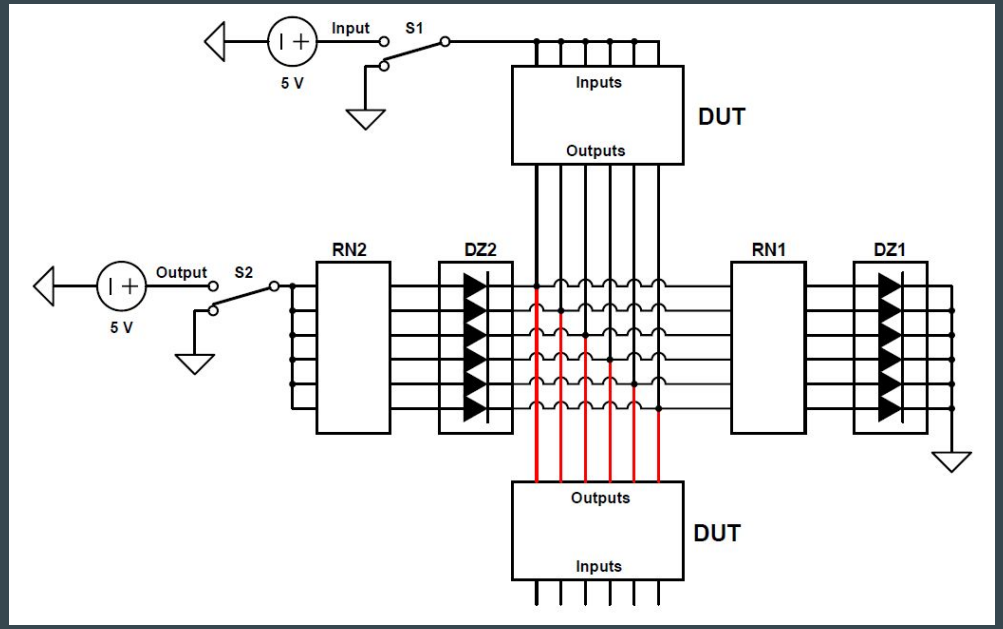
Bussed Resistor Network

Isolated Resistor Network

Burn-in Boards

Issues

2. All output gates of each testing setup are connected with other output gates



Data Analysis

General Procedure

Once the lifetimes of the parts have been collected (and a control group that wasn't stressed) we can pick apart the data.

This will require statistical analysis. After all, no sample is perfectly representative of the parts' entire population.

Our primary statistic of interest will be the mean lifetimes of the parts.

Implications

If Latent Damage does exist, it could cause serious issues for the industry.

Conventional repair procedures could be invalid.

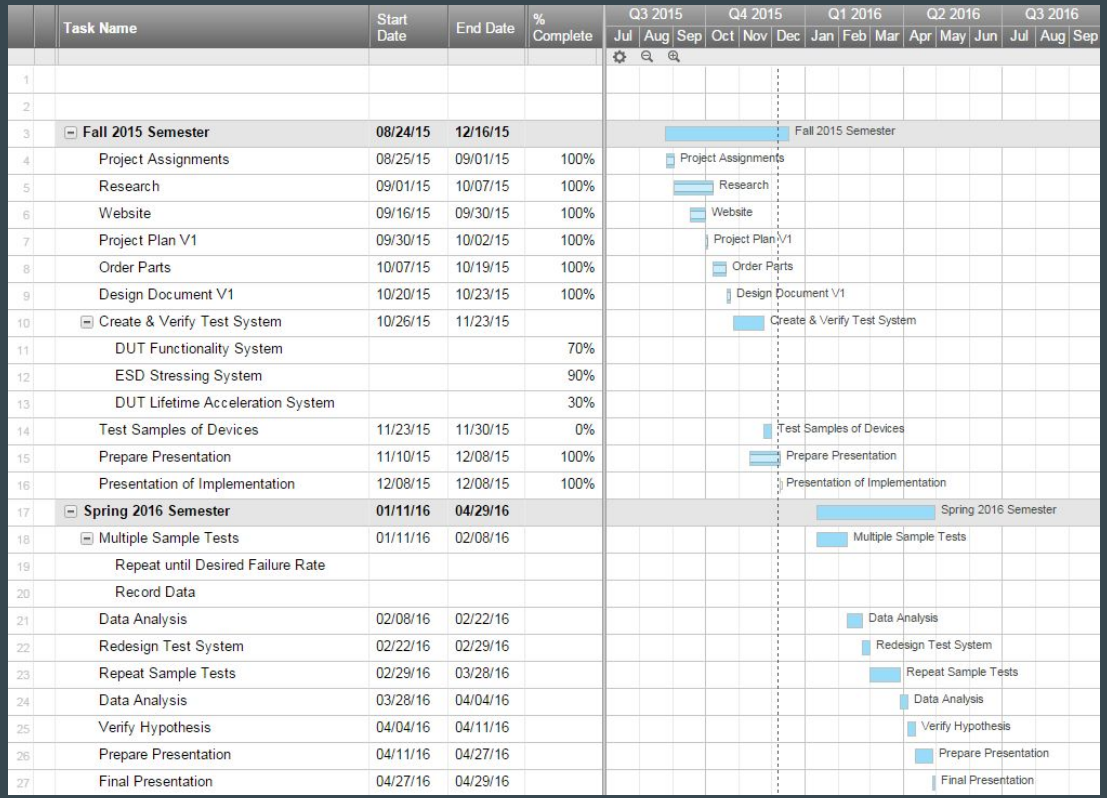
ESD affected systems might need to be completely replaced.

Completed Work

So far, we've done the following toward the completion of the project:

- Replaced high-voltage source
- Began work on establishing a max stress level
- Determined issues and intended operation of existing boards
- Implemented a single-device testing set-up

Project Milestones & Schedule



	Task Name	Start Date	End Date	% Complete
1				
2				
3	**Fall 2015 Semester**	**08/24/15**	**12/16/15**	
4	Project Assignments	08/25/15	09/01/15	100%
5	Research	09/01/15	10/07/15	100%
6	Website	09/16/15	09/30/15	100%
7	Project Plan V1	09/30/15	10/02/15	100%
8	Order Parts	10/07/15	10/19/15	100%
9	Design Document V1	10/20/15	10/23/15	100%
10	Create & Verify Test System	10/26/15	11/23/15	
11	DUT Functionality System			70%
12	ESD Stressing System			90%
13	DUT Lifetime Acceleration System			30%
14	Test Samples of Devices	11/23/15	11/30/15	0%
15	Prepare Presentation	11/10/15	12/08/15	100%
16	Presentation of Implementation	12/08/15	12/08/15	100%
17	**Spring 2016 Semester**	**01/11/16**	**04/29/16**	
18	Multiple Sample Tests	01/11/16	02/08/16	
19	Repeat until Desired Failure Rate			
20	Record Data			
21	Data Analysis	02/08/16	02/22/16	
22	Redesign Test System	02/22/16	02/29/16	
23	Repeat Sample Tests	02/29/16	03/28/16	
24	Data Analysis	03/28/16	04/04/16	
25	Verify Hypothesis	04/04/16	04/11/16	
26	Prepare Presentation	04/11/16	04/27/16	
27	Final Presentation	04/27/16	04/29/16	

Updated on December 7th, 2015

Next Semester Plans

- Establish maximum stress level
- Addressing Burn-in PCB issues
  - Create New PCB Design
  - Implement new components
- Begin Stressing & Burn-in Devices
  - Test Control Group
    - Non-stressed devices
  - Test Experimental Group
    - Stressed devices at maximum stress level
- Analyze Data
  - Hypothesis Testing

Thank you!

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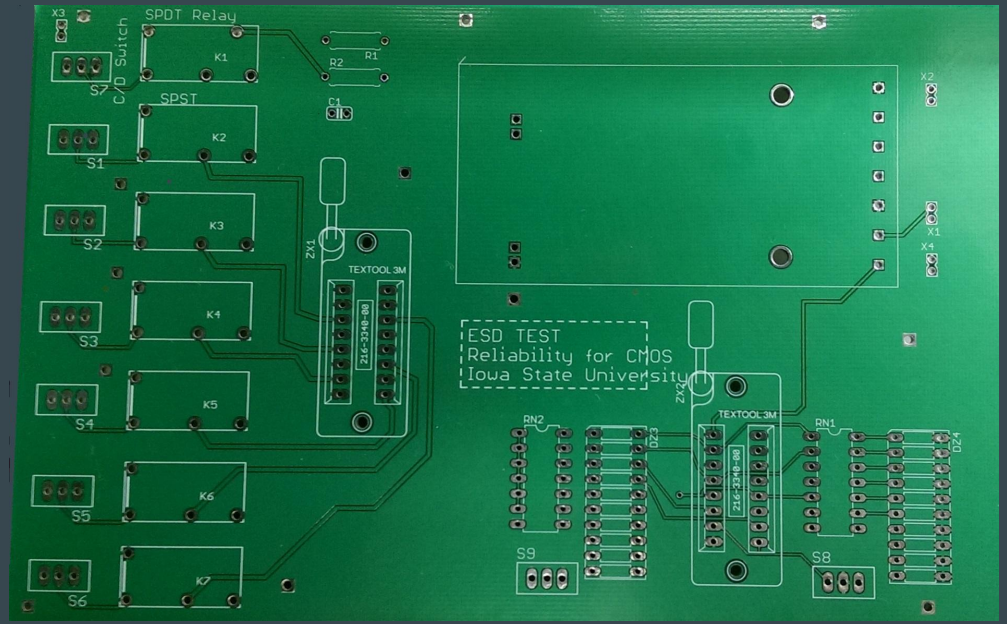
Any Questions?

Resource/Cost Estimate

Bill of Materials					Updated: December 3rd 2015	
Item	Qty.	Reference	Cost	Part Description	Supplier	Supplier #
1	1	M20	$53.49	Fence Energizer (High-voltage source)	Gallagher	M20
2	1	DEFT-Z	$36.37	Digital Electric Fence Tester	Zareba	DEFT-Z
3	50	10M Resistors	$7.88	RES MF HV .25W 10M OHM 1% AXIAL	Digi-Key	RNV14FAL10M0CT-ND
4	10	DHRB34A101M2BB	-	Murata Ceramic Disc Capacitors 100pF +/-20%	Mouser	81-DHRB34A101M2BB
5	500	CD4049UBE	-	TI Hex Inverters	Digi-Key	296-2055-5-ND
6	2	Custom	-	ESD Stress PCB	-	-
7	10	Custom	-	DUT burn-in PCB	-	-
		TOTAL COST	$97.74			

Updated on December 3rd, 2015

ESD Stress PCB



FIT to MTTF

Arrhenius equation:

$$k = Ae^{-(Ea/RT)}$$

- k: Boltzmann's Constant
- A: frequency factor/pre-exponential factor
- Ea: activation energy (eV)
- R: gas constant
- T: temperature (in kelvins)

FIT (Failures In Time) to MTTF (Mean Time To Failure)

$$FIT = \lambda_{FIT} = \lambda_{hours} \times 10^9$$

$$MTTF_{hours} = 1/\lambda_{hours}$$

λ = Failure Rate